Summary of 13th April 2017 Fully-Depleted Silicon-On-Insulator (FD-SOI) Symposium and 14th April 2017 FD-SOI Tutorial/Training events in Santa Clara, CA

With the Mobile Communication industry gradually moving inexorably towards 5G Evolution in mm-Wave frequency spectrum and with numerous other emerging markets requiring silicon-certified low-power high-performance mm-Wave Application-Specific Integrated Circuits (ASICs) and Intellectual Property (IP) development, nanoscale FD-SOI CMOS process technology has suddenly become a very credible alternative to nanoscale Bulk CMOS and Silicon Germanium process technologies. It was thus timely that the SOI Consortium (http://soiconsortium.eu) had organised two keynote FD-SOI events for 13th and 14th April 2017 in Silicon Valley which was attended by Tetrivis. The events are summarised below:

13th April 2017 FD-SOI Symposium Day

Close to 200 people from both industry and academia attended the Symposium Day at Hyatt Regency Hotel, Santa Clara, CA, over the course of the morning and afternoon sessions.

Presentation slides will shortly be available on SOI Consortium website (http://soiconsortium.eu/events/). The various sessions are summarised below:

Morning Session I (SOI Applications and Perspectives)

The first presentation was from NXP, with Geoff Lees, Senior Vice President & General Manager, Microcontrollers, speaking on "*Application of Technology in Embedded Processing*". He contrasted chip scaling vs. chip diversification trend as System-on-Chip (SoC) and System-in-Package (SiP) solutions are architected for **Internet of Things** (IoT), Sensors, Connectivity, Computation and Graphics/Imaging applications. Future Microprocessor (MPU) technology trend was from 40nm to 7nm CMOS, whereas Microcontroller (MCU) technology trend was from 130nm to 40nm (primarily due to Flash memory technology manufacturing limit currently being 40nm CMOS). FD-SOI 28nm CMOS is thus the research and development area for next-generation Memory and manufacture-able Flash Memory. In Geoff's words, FD-SOI has become the "*New Normal*" for ultra-low-power consumption and high performance chipsets with intrinsic on-the-fly optimisation. Notably, NXP presented various **commercially available** ARM-Cortex chipsets that use FD-SOI Forward Body Bias

(FBB) and Reverse Body Bias (RBB) to achieve unprecedented performances at extremely low power consumption levels. They were manufactured using Samsung's 28nm FD-SOI technology (licensed from ST Microelectronics) in Samsung's Fab in South Korea and Austin, TX.

Global Foundries then took to the stage for the second presentation with Alain Mutricy, Senior Vice President, Product Management, speaking on "*FDX™ (FD-SOI) Accelerating Boosting Product Competitiveness in High Growth Markets*". He highlighted the slow-down of the smart phone market and the fact that IoT was becoming a rapidly growing market for semiconductor applications. He mentioned that Global Foundries 22nm FD-SOI Process Design Kit (PDK) version 1.1 was currently available and that 22nm CMOS (bulk or FD-SOI) was the biggest semiconductor battle ground (he showed comparative slides with 22nm Bulk CMOS offerings from both Global Foundries and competitors). Around 40% to 50% lower power consumption was typical between bulk and FD-SOI in the same technology node. Global Foundries also have a road map down to 12nm FD-SOI and are building a new Fab in China (Q2 2019 completion) in addition to their existing Fab in Dresden, Germany. Alain committed publicly to June 2017 availability of mm-Wave-characterised PDK.

Morning Session II (IOT and Market Opportunities)

Samsung was next, with the third presenter being James Stansberry, Senior Vice President & US Head of ARTIK™ Samsung IoT who spoke on "*Next Steps in IoT's Evolution*". He gave a 'futuristic' presentation on how the FD-SOI-enabled IoT landscape can look in the next five or so years with Secure Homes, Pet Care, Wellness, Industrial Manufacturing, Autonomous Vehicles and Big Data analytics being applications that will create the wave on which the adoption of IoT devices will ride. 16 billion connected devices are being forecast for 2031 with connected devices targeted to surpass mobile devices in 2018. He mentioned that IoT today was just automation with smart-phone-based remote control but the future was the **Interoperability of Things**. There are challenges (data security as an example) but this will be surmounted. He talked about Autonomy of Things (Artificial Intelligence has already surpassed humans in both Speech and Image recognition) and how machines are gradually replacing humans even in Health Care and Medical Pathology. He presented Samsung's ARTIK™ interconnectivity platform (Samsung aims to achieve interconnectivity for all their products by 2020) and the need for the industry to work together to define protocols that will allow a Samsung Refrigerator with a display, for example, to work with another company's camera mounted outside the house entrance and yet still be able to aggregate biometrics data from a person's smart watch and seamlessly move it from house to 'autonomous' vehicle. Various videos of these concepts were showcased.

Ron Moore, Vice President, Physical Design Group, ARM was the fourth presenter and he spoke on "*Low Power IP: Essential Ingredients for IoT Opportunities*". Ron mentioned that ARM is poised for fuelling the IP ingredients for IoT (Processor, Radio, Security and Sensor/Actuator) opportunities with 16 billion ARM-based chips shipping in 2016 and 100 billion ARM-based chips forecast for 2017. For high-growth IoT areas, the devices will be off or idle most of the time so extremely low leakage technology is key (Samsung's 28nm FD-SOI technology provides 10 times lower leakage for same performance and 45% higher performance for comparable leakage using RBB when compared to

Bulk CMOS technology in the same process node). ARM is also data security focussed in their processor architectures, with Ron encouraging many more semiconductor companies to develop IPs to fuel IoT growth.

The fifth speaker was Handel Jones, IBS Chief Executive Officer, with his presentation entitled "*Growth Areas for IoT and the Impact of FD-SOI*". He elaborated on how IoT was simply about the monetization of data with key players already in that space being Google and Amazon. He also talked about 3D-NAND Memory and a key technology paradigm shift being Sony's Image Sensor manufactured in TSMC 28nm Bulk CMOS technology. He talked about various IoT applications (Autonomous Driving, Smart-Phone Imaging, Augmented Reality) stressing the fact that 28nm Bulk CMOS technology is high-volume and will remain so for many years to come. As a result, FD-SOI technology needed to show more credibility and cost-effectiveness before it will experience global take-off and adoption. But according to him, FD-SOI Fab prices are coming down and for RF, ultra-low-power, Analogue and Mixed-Signal applications, FD-SOI is the best bet.

Afternoon Session I (IP Ecosystem and Product Innovations)

Synopsys began the afternoon session with the sixth speaker being John Koeter, Synopsys Vice President, Marketing Solutions Group. His presentation was on "*FD-SOI in The Connected World*". He renamed IoT "**Immensely Optimistic Thinking**" and envisioned IoT to encompass all the technologies and products "*from the Edge to the Cloud*" where edge devices were the data sources (sensors, application processors) and the cloud was abstracted data location for post-processing. He touted the concept of "*Connected Cows*" (given he was based in Austin, TX), amongst other IoT applications like Smart Blinds to keep the sun out in arid regions. His opinion was that FD-SOI was a good fit for data pre-processing (at the Edge) given its extremely low power operation, with Automated Driving and Assisted Safety, ADAS (94% US automobile accidents are caused by human error) being a key application. He stated that it took an ecosystem to make FD-SOI successful and that Synopsys Logic Design platforms were FD-SOI ready, with Synopsys FD-SOI IP portfolio growing by the day.

Megachip Chief Marketing Officer, Maurizio Paganini, gave the seventh presentation on "*IoT unique identity overlooked*". From his point of view, IoT was a "*fragmented sets of verticals*", "*a social and not a capitalist market*", "*a market of makers and not thinkers or doers*" and "*a true representation of Engineering perfection*". He also mentioned that IoT must be energy-neutral, cheap, secure and completely pervasive to be successful and IoT deep-sleep mode can be used to enhance security.

The eighth presenter was Jens Benndorf, Chief Operating Officer of Dreamchip. This was the only company at the symposium that had test silicon results from Global Foundries 22nm FD-SOI technology. His presentation was titled "*A new Computer Vision Processor Chip Design for Automotive ADAS CNN Applications in 22nm FD-SOI*" and described an image processor chip that could acquire and stitch image streams from up to four cameras to create a wide-angle panoramic composite image, which can be used in automobiles to render panoramic blind-spot-free images behind and around the car when conventional mirrors are replaced with digital cameras. This will significantly improve pedestrian detection and reduce blind-spot-related accidents. They have received and tested first silicon and did a second tape-out in January 2017. Chip supports 4GB DDR4

Memory, had four HDMI inputs and consumed 3W to 5W (with the main processor running at 1GHz and image processor running at 300MHz).

Greenwaves' Chief Executive Office, Loic Lietar was the ninth presenter and talked about "*High performance ultra-low power parallel IoT processor architecture: Leveraging FD-SOI*". He broke down IoT related tasks to three: Sense, Classify/Analyse and Communicate. Given the "*16 Zettabytes (10^{21} bytes) of internet data that has been generated in 2017 so far of which a large proportion of it was video or images* [presenter 3]", it was important for the "*Edge*" device to have sufficient intelligence to sift through and classify large datasets whilst only transmitting or communicating the lower bit-rate decisions or interrupt flags. Greenwaves experienced a 4.5x consumption reduction for same performance in their 55nm Bulk CMOS chip versus their 28nm FD-SOI CMOS chip. The Greenwaves chip can classify a quality QVGA image every three minutes for 10 years on a 3.6Ah battery.

To round off the afternoon session, Marie-Noelle Semeria, Chief Executive Officer of CEA-Leti did the tenth presentation on "*FD-SOI factors of success pave new roadmaps*". She reported device F_{MAX} of as high as 390GHz in ST Microelectronics 28nm FD-SOI technology (CEA-Leti produced the models that ST Microelectronics bundle with their PDK with extremely good correlation with measurement demonstrated during the 14th April Tutorial/Training event). FD-SOI thus opens the door for unusual nanoscale semiconductor applications i.e. Quantum Computing, Nanosystems and Photonics (very efficient photodiodes have been made using the technology and can co-exist with the usual NMOS and PMOS devices).

Panel Session (Design-Technology Ecosystem Readiness)

The following panellists were then invited on stage and fielded a number of prepared questions from Adele Hars, (Editor in Chief of Advanced Substrate News, ASN) and a few from the floor.

- Wayne Dai, CEO, Verisilicon
- Samuel George, Sr. Director, GLOBALFOUNDRIES
- John Koeter, VP Marketing Solutions, Synopsys
- Jayanta Lahiri, VP, Invecas
- Kelvin Low, Sr. Director, Samsung
- Christophe Maleville, EVP&GM, Digital, Soitec
- Ron Moore, VP, Physical Design Group, ARM
- Samir Patel, CEO, Sankalp Semiconductor

The general consensus was that despite the fact that 28nm FD-SOI CMOS technology came seven years after 28nm Bulk CMOS technology, FD-SOI was now ready for IoT and mm-Wave applications with the industry slowly and surely growing chipset and IP ecosystem to fuel this growth. Many companies are choosing FD-SOI rather than rival Fin-FET technology primarily due to mask set costs. FD-SOI also offers seamless performance vs. consumption trade-off via Body Bias leveraging, where the trade-off decision point can be taken before tape-out (hard body bias) or on fabricated silicon (configurable body bias).

14th April 2017 FD-SOI Tutorial/Training Day

The Tutorial event was held at Samsung's offices in Santa Clara, CA and close to 100 people attended. The presentations were technical in nature and each lasted for about 55 minutes with 5 minutes for questions. All five presenters were then invited back on stage at the end to field questions from the floor. FD-SOI circuit design techniques were extensively discussed with measured results presented and silicon performance showcased up to mm-Wave frequencies. Samsung and ST Microelectronics 28nm FD-SOI technology was more mature and better characterised than Global Foundries 22nm FD-SOI, but Global Foundries were working hard to get to a decent level of maturity as well for mm-Wave applications.

- Andreia Cathelin, Fellow, STMicroelectronics Crolles, France; "*FDSOI short overview and advantages for analog, RF and mmW design*"
- Sorin Voinigescu, Professor, University of Toronto, Toronto, Canada; "*Unique circuit topologies and back-gate biasing scheme for RF, mm-wave and broadband circuit design in FDSOI technologies*"
- Joachim Rodrigues, Professor, Lund University, Lund, Sweden; "*Design strategies for ULV memories in 28nm FDS-SOI*"
- Bora Nikolic, Professor, UC Berkeley, Berkeley, USA; "*Energy-Efficient Processors in 28nm FDSOI*"
- Boris Murmann, Professor, Stanford University, Palo Alto, USA; "*Pushing the envelope in mixed-signal design using FD-SOI*"