Tetrivis

TRV001TSM40LP Logic Requirements

Revision 1.1

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Revision History

Revision	Change Description	Date	Author
1.0	First Draft	12th December 2014	Olujide ADENIRAN
1.1	Updated with additional information	21st January 2015	Olujide ADENIRAN

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1 Abbreviations and References

1.1 Abbreviations

ADC	Analogue to Digital Converter
DAC	Digital to Analogue Converter
DEM	Dynamic Element Matching
IP	Intellectual Property
PLL	Phase Locked Loop
RTL	Register Transfer Level
SFDR	Spurious-Free Dynamic Range
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio

1.2 References

2 Introduction

TRV001TSM40LP is a Test Chip currently being designed by Tetrivis in TSMC 40nm CMOS process technology. It comprises the TRV101TSM40LP (12-bit ADC IP), the TRV201TSM40LP (12-bit DAC IP) and the TRV301TSM40LP (Fractional-N PLL IP). The ADC, DAC, PLL and Test Chip have associated digital cores for control, calibration, frequency division and signal processing functions. These logic subsystems have been written in RTL (TRV101TSM40LP, TRV301TSM40LP) and gate-level (TRV001TRM40LP, TRV201TSM40LP) by Tetrivis and it is desired to synthesis, time-analyse and carry out placement and routing of the logic subsystems, with final deliverables being hard macro GDSII, timing files, synthesized Verilog code and Spice netlist of each of the four logic subsystems.

All gate count estimates were based on post-synthesis results of synthesis procedure carried out using freeware synthesis tools and a vanilla CMOS technology. Area estimates were then derived by using actual TSMC 40LP standard cell library gate area to multiply the post-synthesis gate counts, with the total number marked up by 50% to factor in routing overheads. Metal-4 and below should be used for routing.

2.1 Document Scope

This document details the RTL requirements for the four logic cores present in the TRV001TSM40LP test chip and is intended to aid quotation preparation and design implementation.

3 TRV301TSM40LP Logic Core Requirements

The TRV301TSM40LP_digicore block comprises PLL calibration engine and Fractional-N ΔΣ modulator. Given that the PLL analogue layout design is complete, this block will be the first to be implemented. Table 3.1 below detail the logic subsystem requirements. Implementation Shape perimeter is subject to change. RTL file is supplied by Tetrivis.

Table 3.1 TRV301TSM40LP Logic Core Requirements

Logic Subsystem	TRV301TSM40LP_digicore
Input Pin Count	38
Output Pin Count	26
Total Pin Count	74
Number of Clock Domains	2 (Crystal Reference and PLL Feedback Inputs)
Maximum Clock Speed	40MHz (Reference) and 40MHz (Feedback)
Gate Count Estimate	6459 gates
Area Estimate	3617 sq-µm
Implementation Shape (LEF supplied)	Rectangular (50.31µm × 69.72µm)
Load Capacitance on Outputs	100fF
Logic Library Flavour (worst-case)	tcbn40lpbwp12tm1phvtwcl0d990d99.lib
Logic Library Flavour (typical-case)	tcbn40lpbwp12tm1phvttc.lib
Logic Library Flavour (best-case)	tcbn40lpbwp12tm1phvtml1d211d21.lib
Allowed Routing Metal Layers	M1 to M4 only (5x-2z-RDL Metal Stack)

4 TRV201TSM40LP Logic Core Requirements

The TRV201TSM40LP_digicore block comprises DAC data-path logic. Table 4.1 below detail the logic subsystem requirements. Implementation Shape perimeter is subject to change. Gate-level netlist file is supplied by Tetrivis.

Table 4.1 TRV201TSM40LP Logic Core Requirements

Logic Subsystem	TRV201TSM40LP_digicore
Input Pin Count	19
Output Pin Count	90
Total Pin Count	109
Number of Clock Domains	1
Maximum Clock Speed	400MHz
Gate Count Estimate	3652 gates
Area Estimate	2045 sq-µm
Implementation Shape (LEF supplied)	Square (45.22µm × 45.22µm)
Load Capacitance on Outputs	100fF
Logic Library Flavour (worst-case)	tcbn40lpbwp12tm1pwcl0d990d99.lib
Logic Library Flavour (typical-case)	tcbn40lpbwp12tm1ptc.lib
Logic Library Flavour (best-case)	tcbn40lpbwp12tm1pml1d211d21.lib
Allowed Routing Metal Layers	M1 to M4 only (5x-2z-RDL Metal Stack)

5 TRV101TSM40LP Logic Core Requirements

The TRV101TSM40LP_digicore block comprises ADC calibration, convergence and data-path logic. Table 5.1 below detail the logic subsystem requirements. Implementation Shape perimeter is subject to change. RTL file is supplied by Tetrivis.

Table 5.1 TRV101TSM40LP Logic Core Requirements

Logic Subsystem	TRV101TSM40LP_digicore
Input Pin Count	17
Output Pin Count	70
Total Pin Count	87
Number of Clock Domains	2 (Sample Clock and Successive Approx. Clock)
Maximum Clock Speed	80MHz (Sample) and 1.6GHz (Successive Approx)
Gate Count Estimate	4717 gates
Area Estimate	2641 sq-µm
Implementation Shape (LEF supplied)	Square (51.39µm × 51.39µm)
Load Capacitance on Outputs	100fF
Logic Library Flavour (worst-case)	tcbn40lpbwp12tm1pwcl0d990d99.lib
Logic Library Flavour (typical-case)	tcbn40lpbwp12tm1ptc.lib
Logic Library Flavour (best-case)	tcbn40lpbwp12tm1pml1d211d21.lib
Allowed Routing Metal Layers	M1 to M4 only (5x-2z-RDL Metal Stack)

6 TRV001TSM40LP Logic Core Requirements

The TRV001TSM40LP_digicore block comprises SPI interface and programmable registers. Table 6.1 below detail the logic subsystem requirements. Implementation Shape perimeter is subject to change. Gate-level netlist file is supplied by Tetrivis.

Table 6.1 TRV001TSM40LP Logic Core Requirements

Logic Subsystem	TRV001TSM40LP_digicore
Input Pin Count	36
Output Pin Count	130
Total Pin Count	166
Number of Clock Domains	1
Maximum Clock Speed	40MHz
Gate Count Estimate	7277 gates
Area Estimate	4075 sq-µm
Implementation Shape (LEF supplied)	Square (63.84µm × 63.84µm)
Load Capacitance on Outputs	100fF
Logic Library Flavour (worst-case)	tcbn40lpbwp12tm1phvtwcl0d990d99.lib
Logic Library Flavour (typical-case)	tcbn40lpbwp12tm1phvttc.lib
Logic Library Flavour (best-case)	tcbn40lpbwp12tm1phvtml1d211d21.lib
Allowed Routing Metal Layers	M1 to M4 only (5x-2z-RDL Metal Stack)